FIG.1

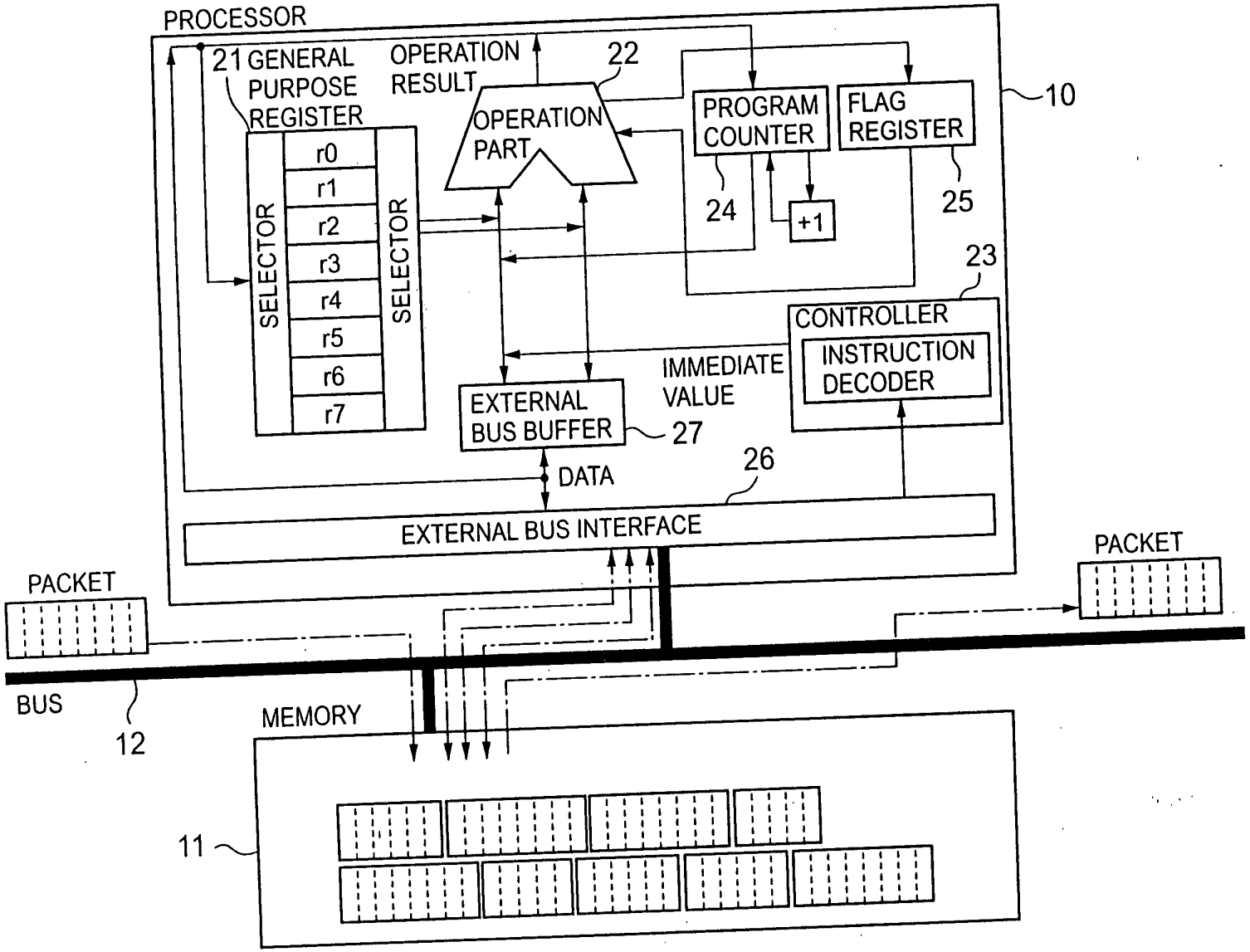


FIG.2

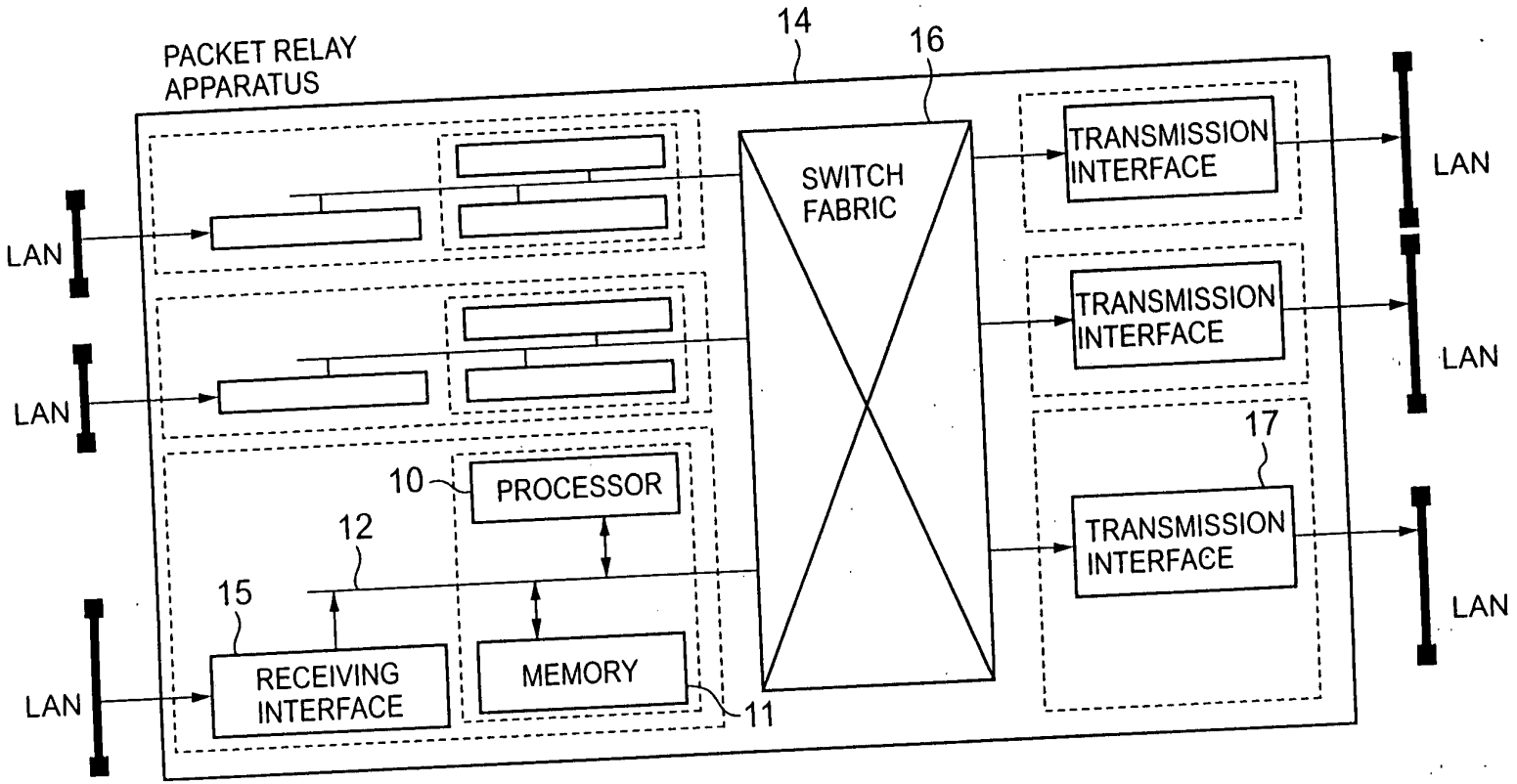


FIG.3

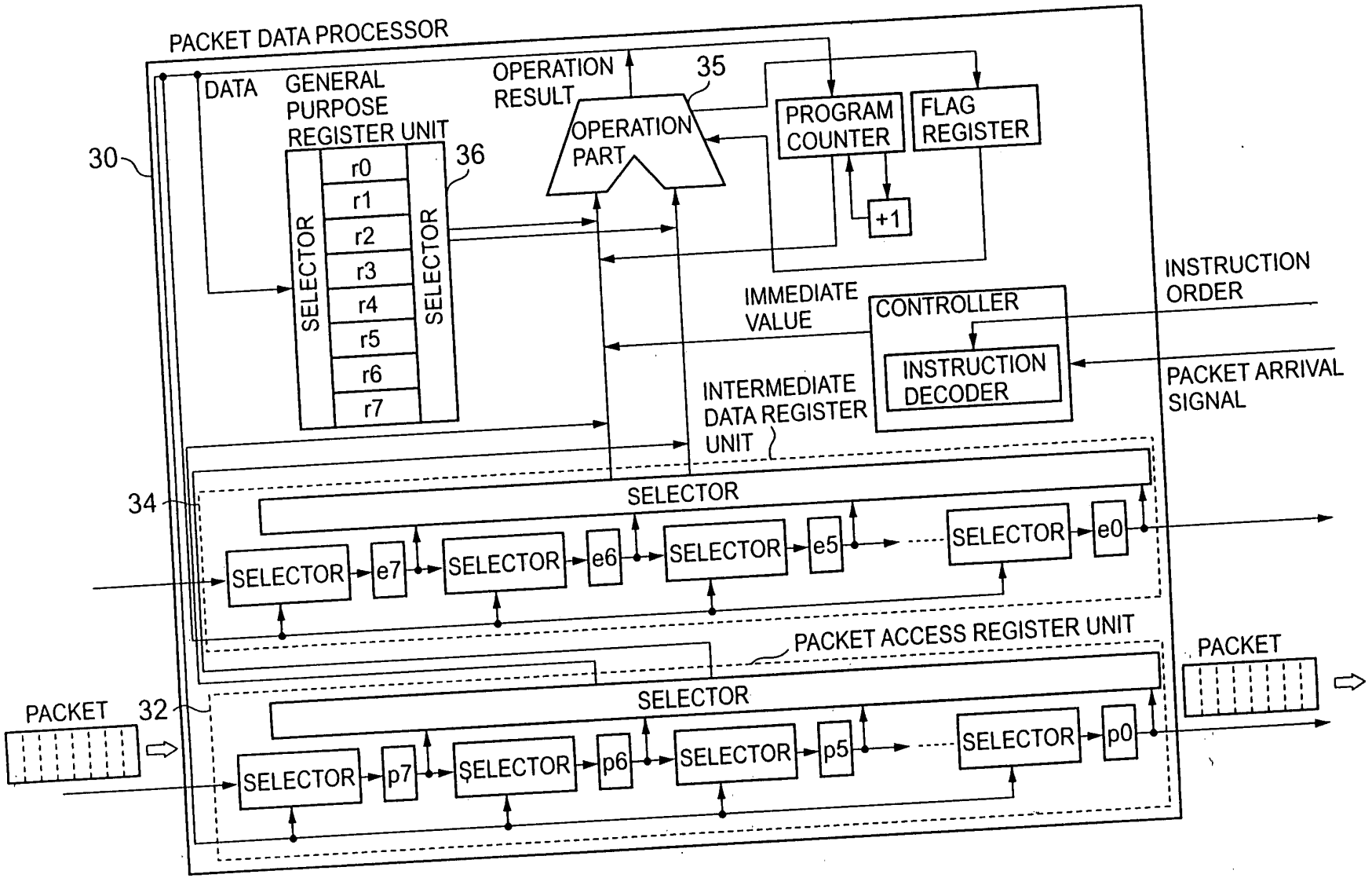


FIG.4A

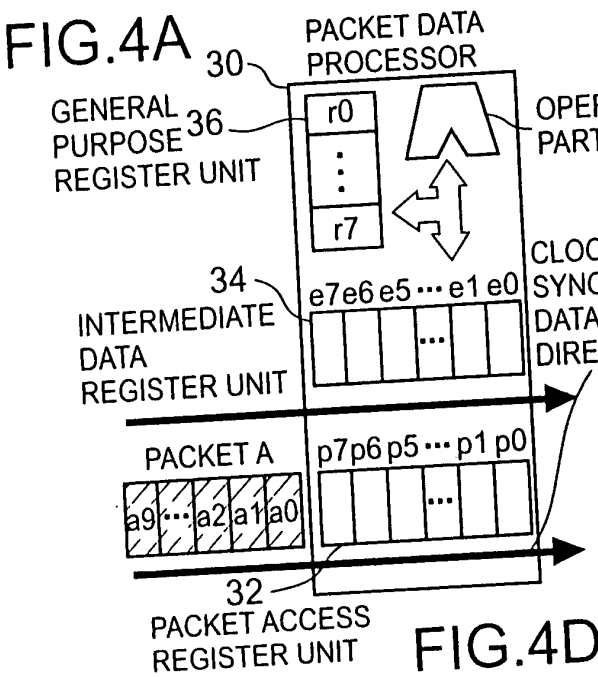


FIG.4B

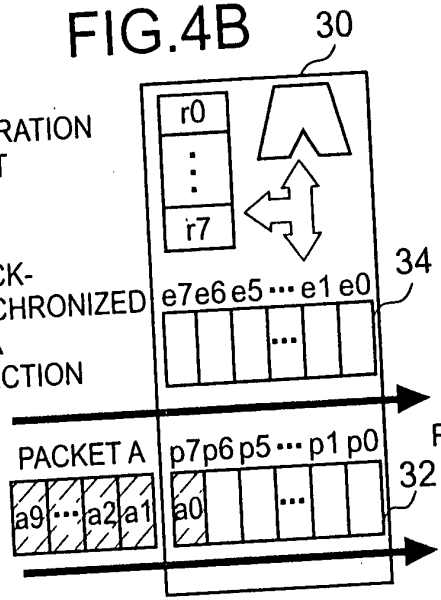


FIG.4C

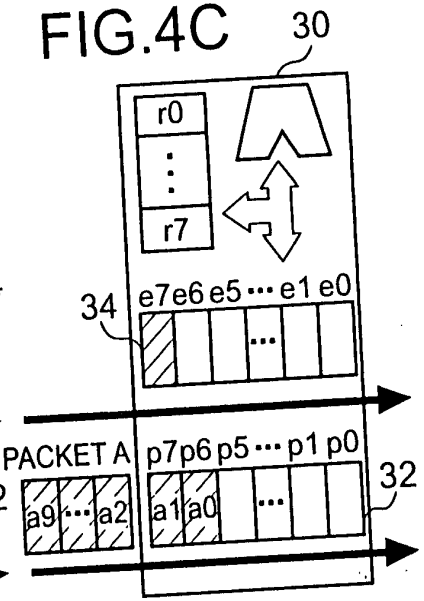


FIG.4D

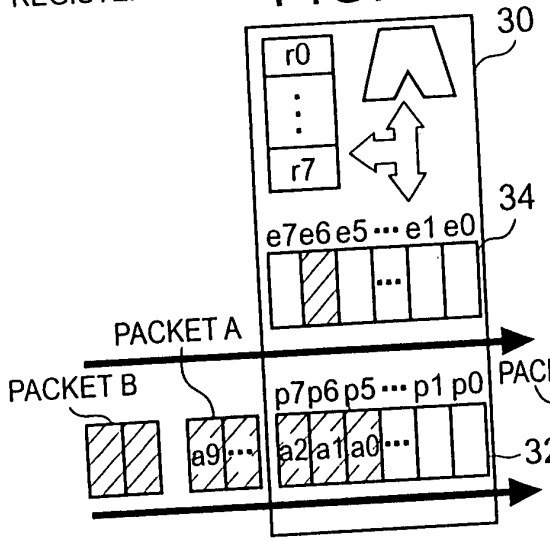


FIG.4E

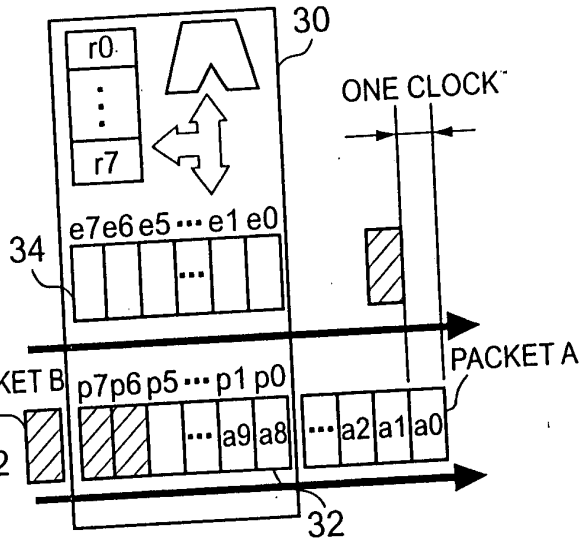


FIG.5

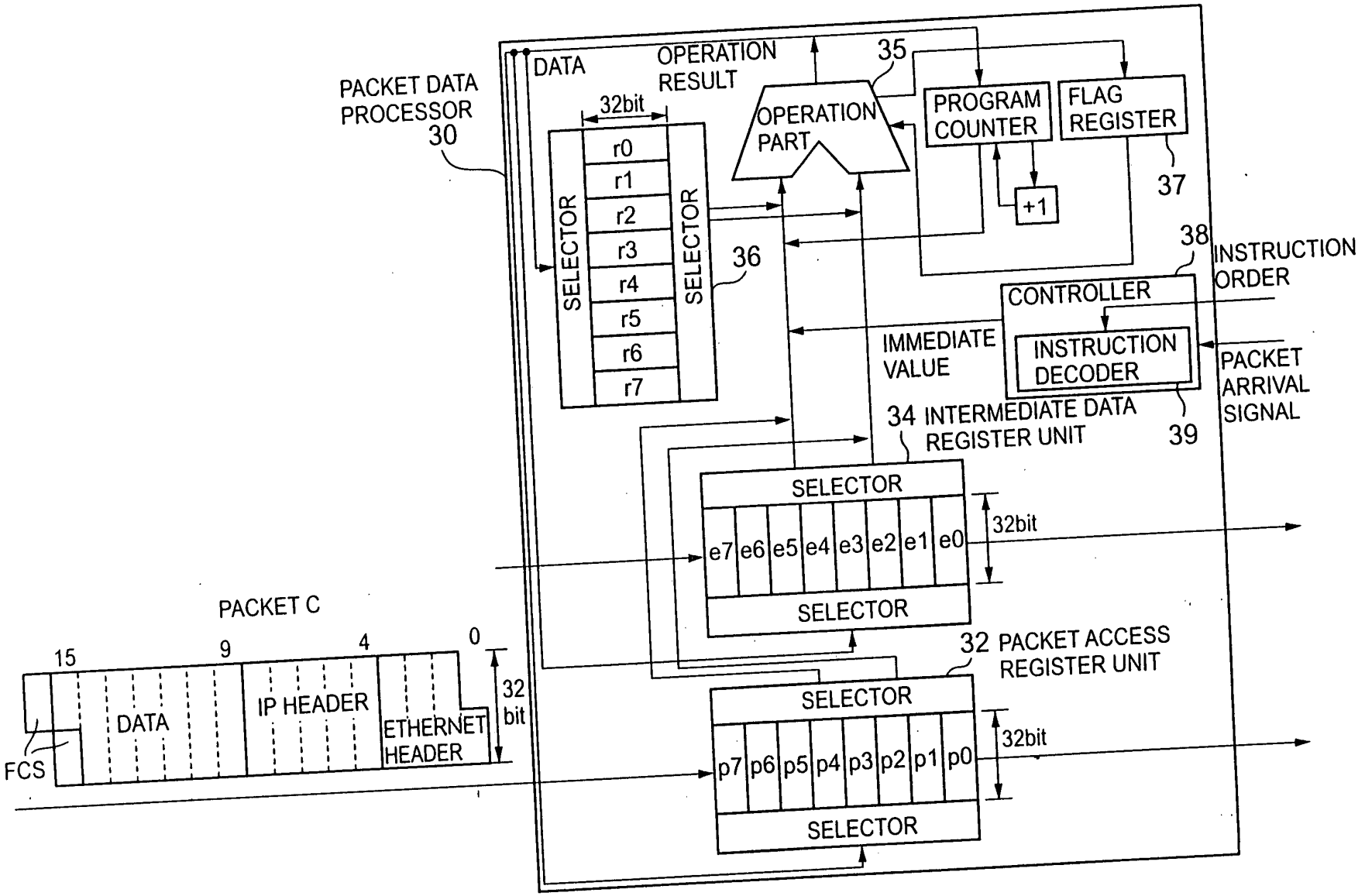


FIG.6

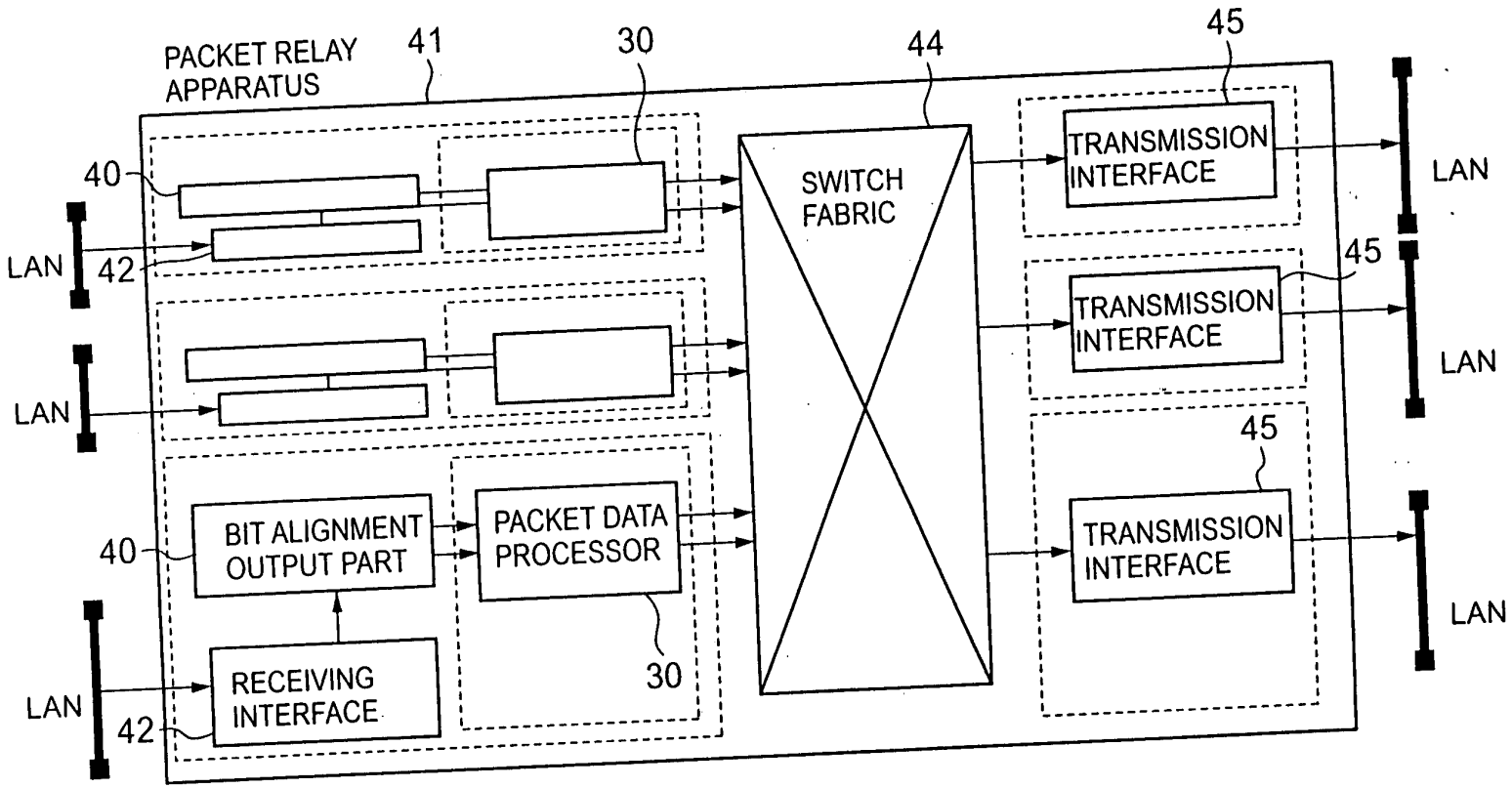


FIG.7

INSTRUCTION TYPE	MNEMONIC INSTRUCTION	OPERATION
NO OPERATION	NOP	No operation but just clock is executed
DATA TRANSMISSION	MOVE	Move word between registers or memories
	MOVW	Move lower word (lower bits) between registers
	MOVB	Move lower byte (lower bits) between registers
ARITHMETIC OPERATION	ADD	Add word integers
	ADC	Add carry and word integer
	ADW	Add lower word
	AWC	Add lower word and carry
	SUB	Subtract word integer
	SBW	Subtract lower word
LOGICAL OPERATION	OR	OR operation of word
	AND	AND operation of word
	XOR	Exclusive-OR operation of word
	NOT	NOT (inverse) operation of word
	NTW	NOT (inverse) operation of lower word and no operation of upper word
	NTB	NOT (inverse) operation by byte
	SFL	Shift left to upper byte and fill 0 to lower byte
	ROTL	Rotate to left
	SFR	Shift right to lower byte and fill 0 to upper byte
	ROTR	Rotate to right
BIT OPERATION	BSF	Get first bit '1' position from lower most bit of source operand
	BSR	Get first bit '1' position from upper most bit of source operand
	BT	Offset bit of source operand 2 based on source operand 1. Set result bit to carry flag of flag register.

FIG. 8

ORDER NUMBER	INSTRUCTION	SECTION WHICH OF PACKET C IS STORED IN PACKET ACCESS REGISTER UNIT							
		p7	p6	p5	p4	p3	p2	p1	p0
1	ANOP	c0							
2	ANOP	c1	c0						
3	ANOP	c2	c1	c0					
4	ANOP	c3	c2	c1	c0				
5	AMOVE r0 p7	c4	c3	c2	c1	c0			
6	AADD r0 r0 p7	C5	c4	c3	c2	c1	c0		
7	AADC r0 r0 p7	c6	c5	c4	c3	c2	c1	c0	
8	AADC r0 r0 p7	c7	c6	c5	c4	c3	c2	c1	c0
9	AADC r0 r0 p7	c8	c7	c6	c5	c4	c3	c2	c1
10	AADC r0 r0 $0	c9	c8	c7	c6	c5	c4	c3	c2
11	AMOVE r1 r0	c10	c9	c8	c7	c6	c5	c4	c3
12	ASFR r0 r0 $16	c11	c10	c9	c8	c7	c6	c5	c4
13	AADW r0 r0 r1	c12	c11	c10	c9	c8	c7	c6	c5
14	ANTW r0 r0	c13	c12	c11	c10	c9	c8	c7	c6
15	≠MOVE e0 $1	c14	c13	c12	c11	c10	c9	c8	c7

FIG.9

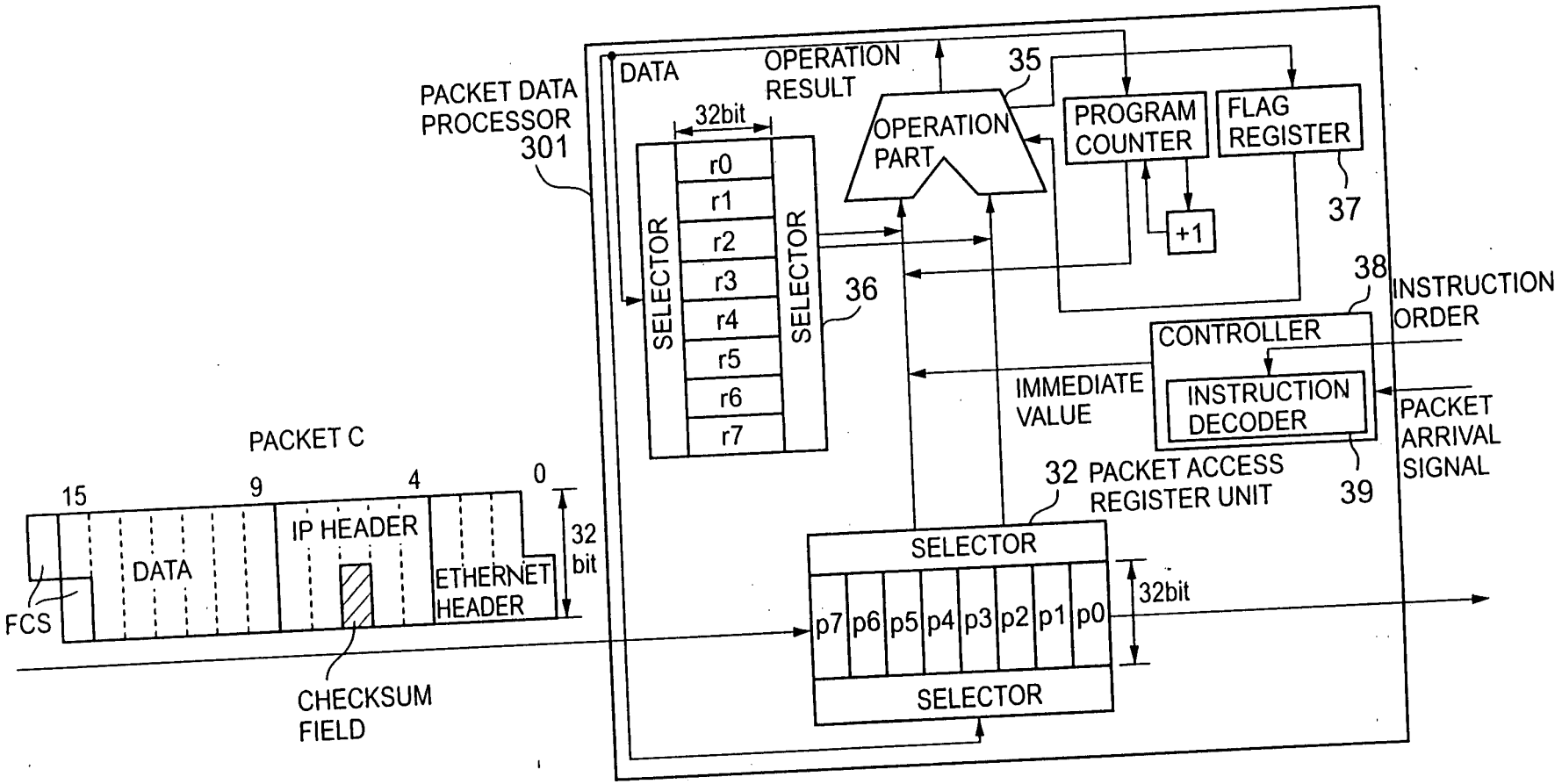


FIG.10

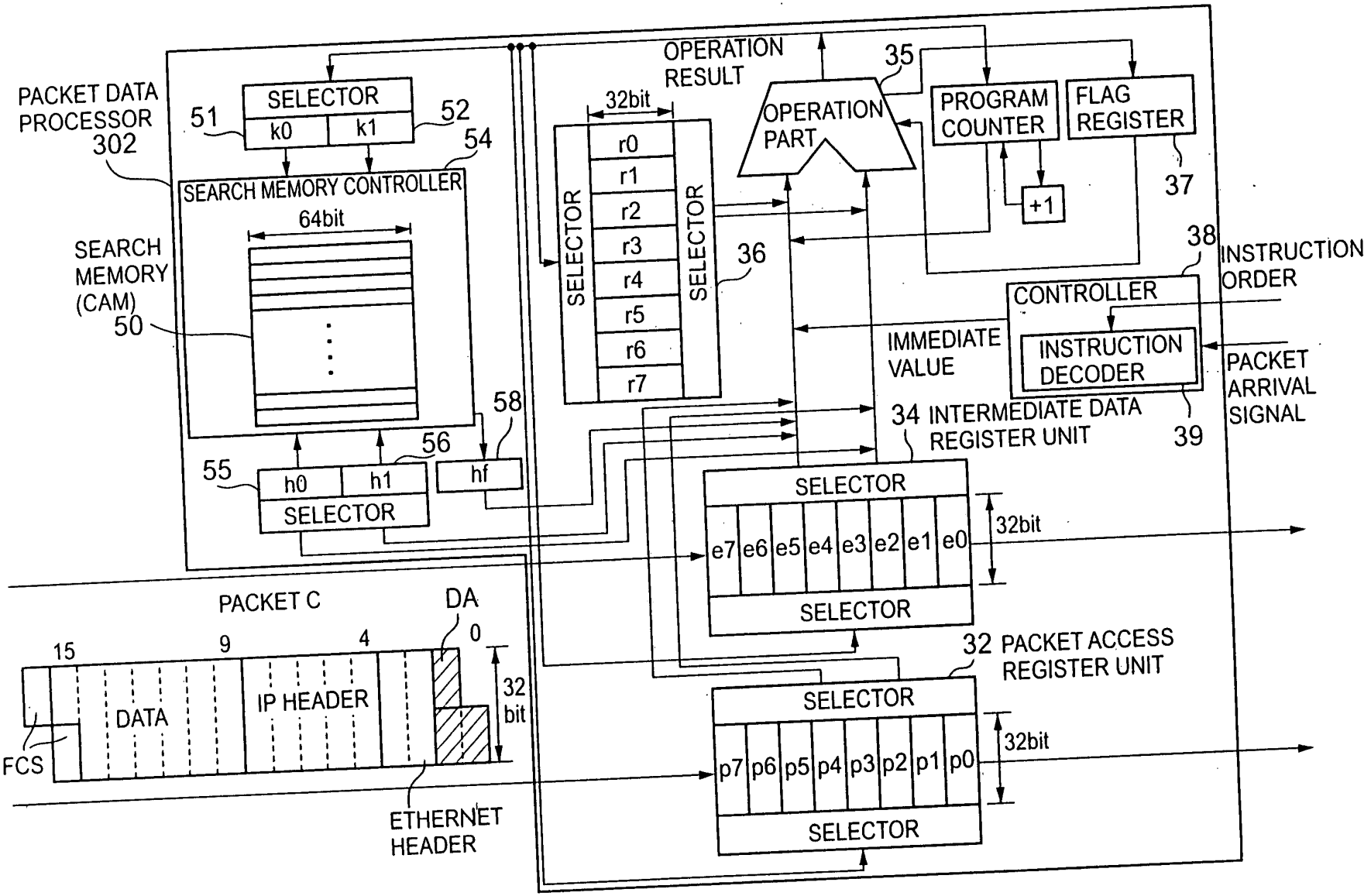


FIG.11

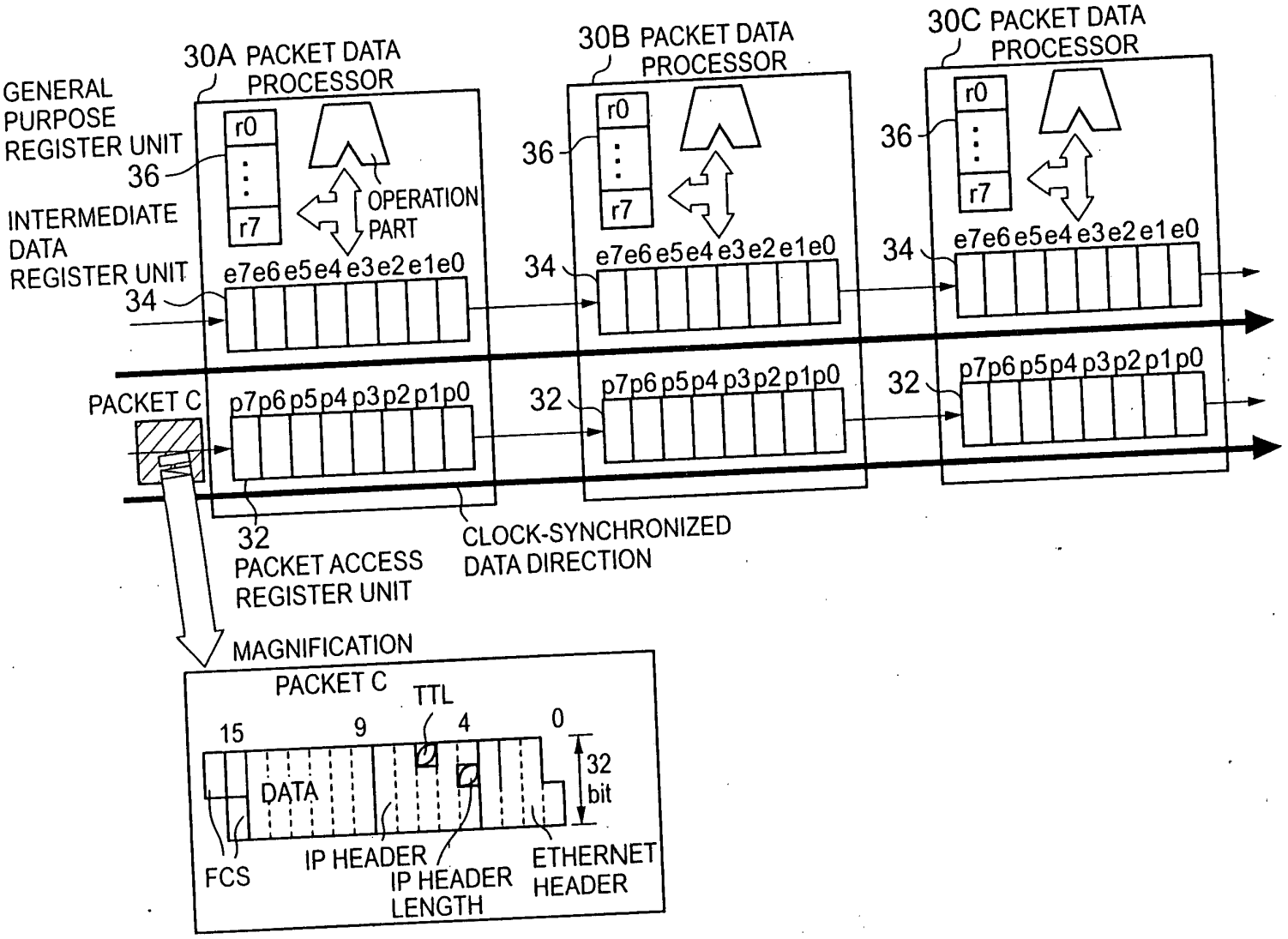

30A PACKET DATA PROCESSOR
30B PACKET DATA PROCESSOR
30C PACKET DATA PROCESSOR
GENERAL PURPOSE REGISTER UNIT
36
r0
r7
OPERATION PART
INTERMEDIATE DATA REGISTER UNIT
34
e7e6e5e4e3e2e1e0
PACKET C
p7p6p5p4p3p2p1p0
32
32 PACKET ACCESS REGISTER UNIT
CLOCK-SYNCHRONIZED DATA DIRECTION
MAGNIFICATION
PACKET C
TTL
15
9
4
0
DATA
32 bit
FCS
IP HEADER
IP HEADER LENGTH
ETHERNET HEADER

FIG. 12

SER. NO	INSTRUCTION ORDER OF PACKET DATA PROCESSOR 30A		INSTRUCTION ORDER OF PACKET DATA PROCESSOR 30B		INSTRUCTION ORDER OF PACKET DATA PROCESSOR 30C	
	ORDER NUMBER	INSTRUCTION	ORDER NUMBER	INSTRUCTION	ORDER NUMBER	INSTRUCTION
1	1	ANOP				
2	2	AMOVE r1 $0				
3	3	ANOT r1 r1				
4	4	ASFR r1 r1 $24				
5	5	ASFR r1 p7 $16				
6	6	AAND r0 r0 r1				
7	7	ASUB r0 r0 $5				
8	8	<MOVE e3 $1				
9			1	ANOP		
10			2	ANOP		
11			3	ANOP		
12			4	ANOP		
13			5	AMOVE r0 p7		
14			6	AADD r0 r0 p7		
15			7	AADC r0 r0 p7		
16			8	AADC r0 r0 p7		
17			9	AADC r0 r0 p7	1	ANOP
18			10	AADC r0 r0 $0	2	ANOP
19			11	AMOVE r1 r0	3	ANOP
20			12	ASFR r0 r0 $16	4	AMOVE r3 $0
21			13	AADW r0 r0 r1	5	ANOT r3 r3
22			14	ANTW r0 r0	6	ASFR r3 r3 $8
23			15	≠MOVE e0 $1	7	AMOVE r0 p7
24					8	ASFR r1 r0 $24
25					9	ASUB r1 r1 $1
26					10	=MOVE e3 $1
27					11	ASFL r1 r1 $24
28					12	AAND r0 r0 r3
29					13	AADD p0 r1 r0

FIG.13

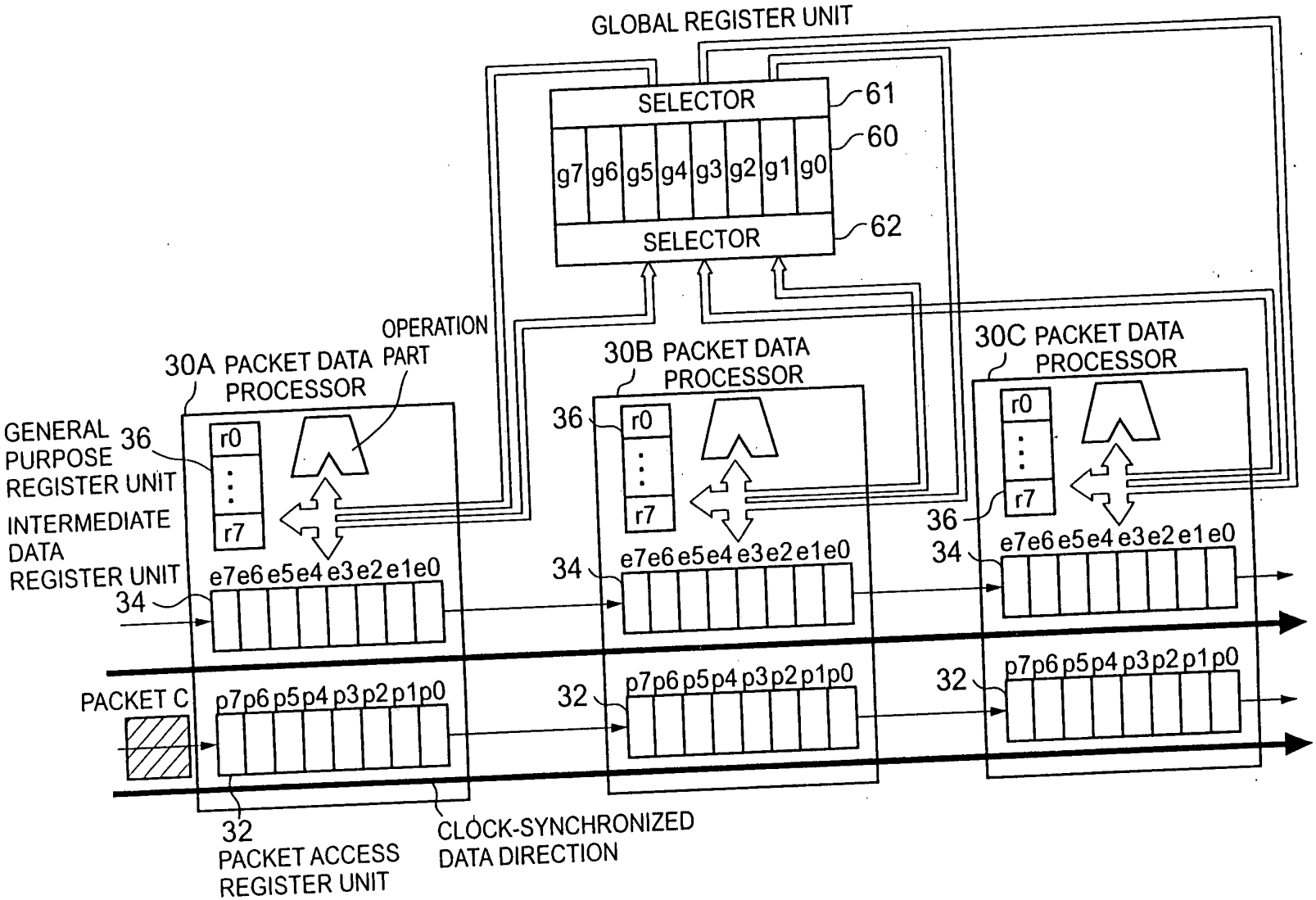


FIG.14

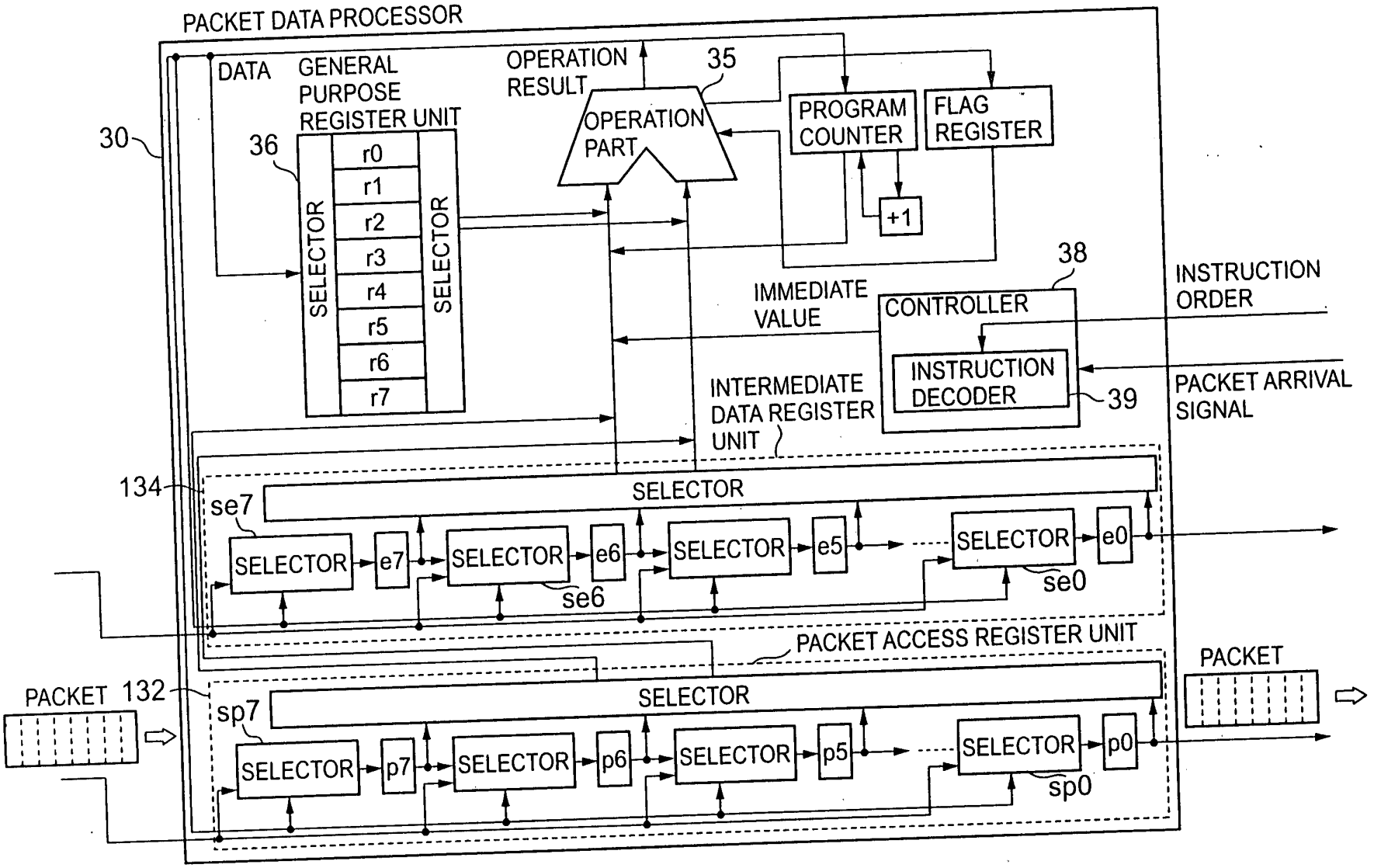


FIG.15

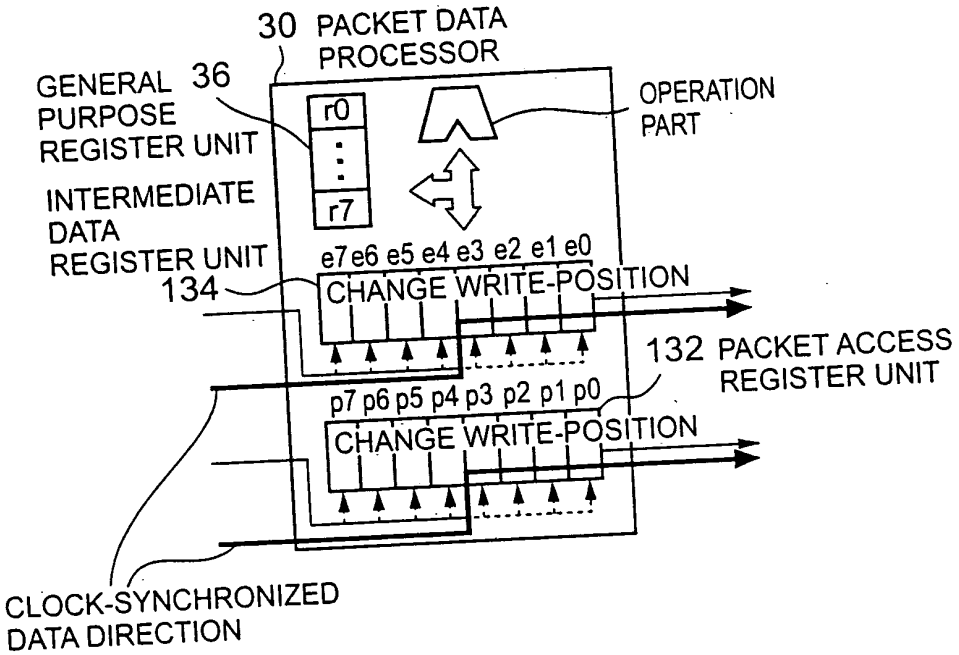

30 PACKET DATA PROCESSOR
GENERAL PURPOSE REGISTER UNIT 36
r0
r7
OPERATION PART
INTERMEDIATE DATA REGISTER UNIT 134
e7 e6 e5 e4 e3 e2 e1 e0
CHANGE WRITE-POSITION
132 PACKET ACCESS REGISTER UNIT
p7 p6 p5 p4 p3 p2 p1 p0
CHANGE WRITE-POSITION
CLOCK-SYNCHRONIZED DATA DIRECTION

FIG.16

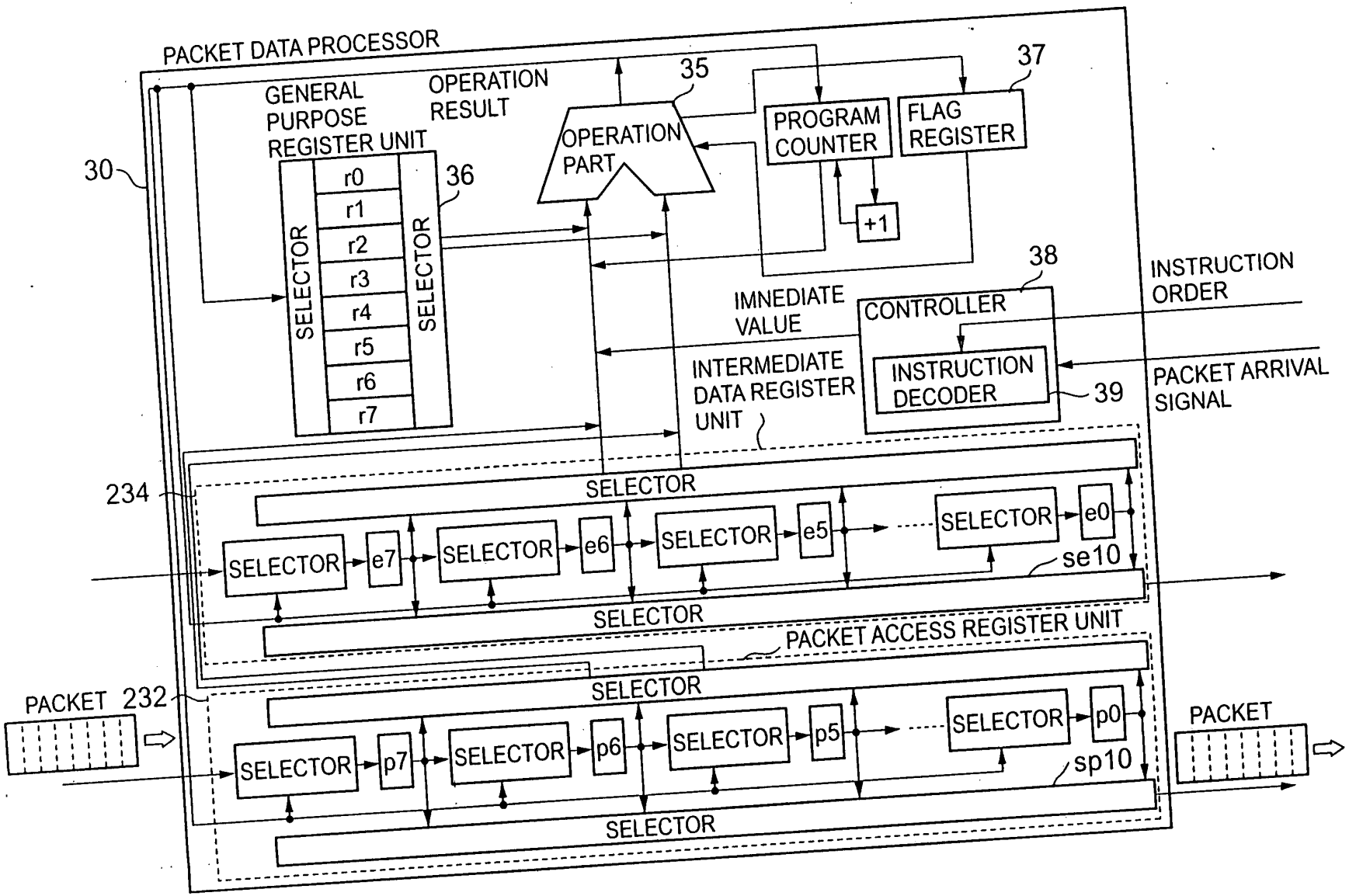
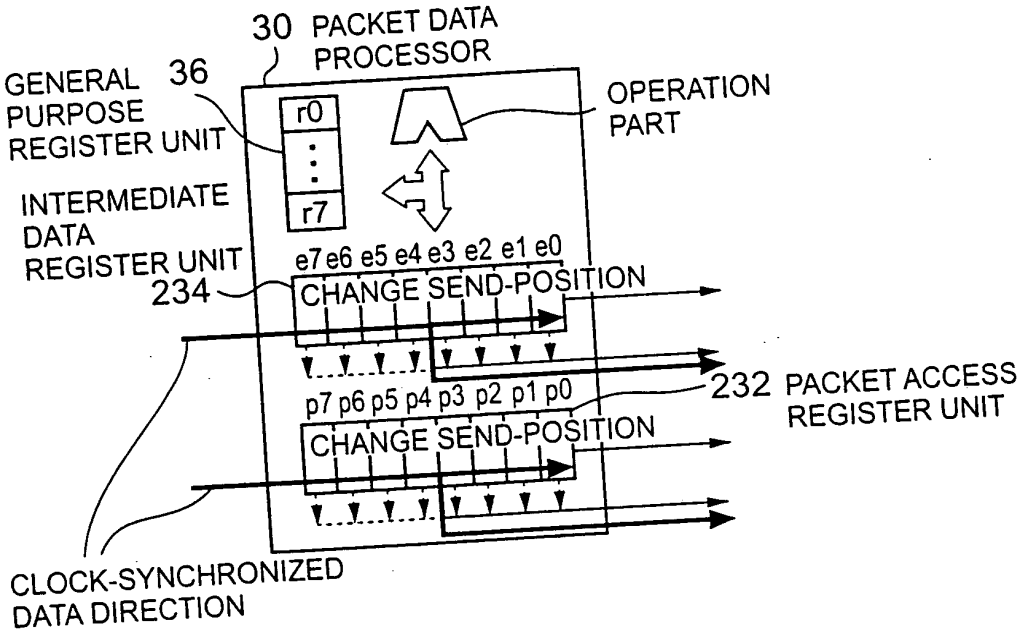


FIG.17


30 PACKET DATA PROCESSOR
GENERAL PURPOSE REGISTER UNIT
36
r0
r7
OPERATION PART
INTERMEDIATE DATA REGISTER UNIT
234
e7 e6 e5 e4 e3 e2 e1 e0
CHANGE SEND-POSITION
p7 p6 p5 p4 p3 p2 p1 p0
CHANGE SEND-POSITION
232 PACKET ACCESS REGISTER UNIT
CLOCK-SYNCHRONIZED DATA DIRECTION